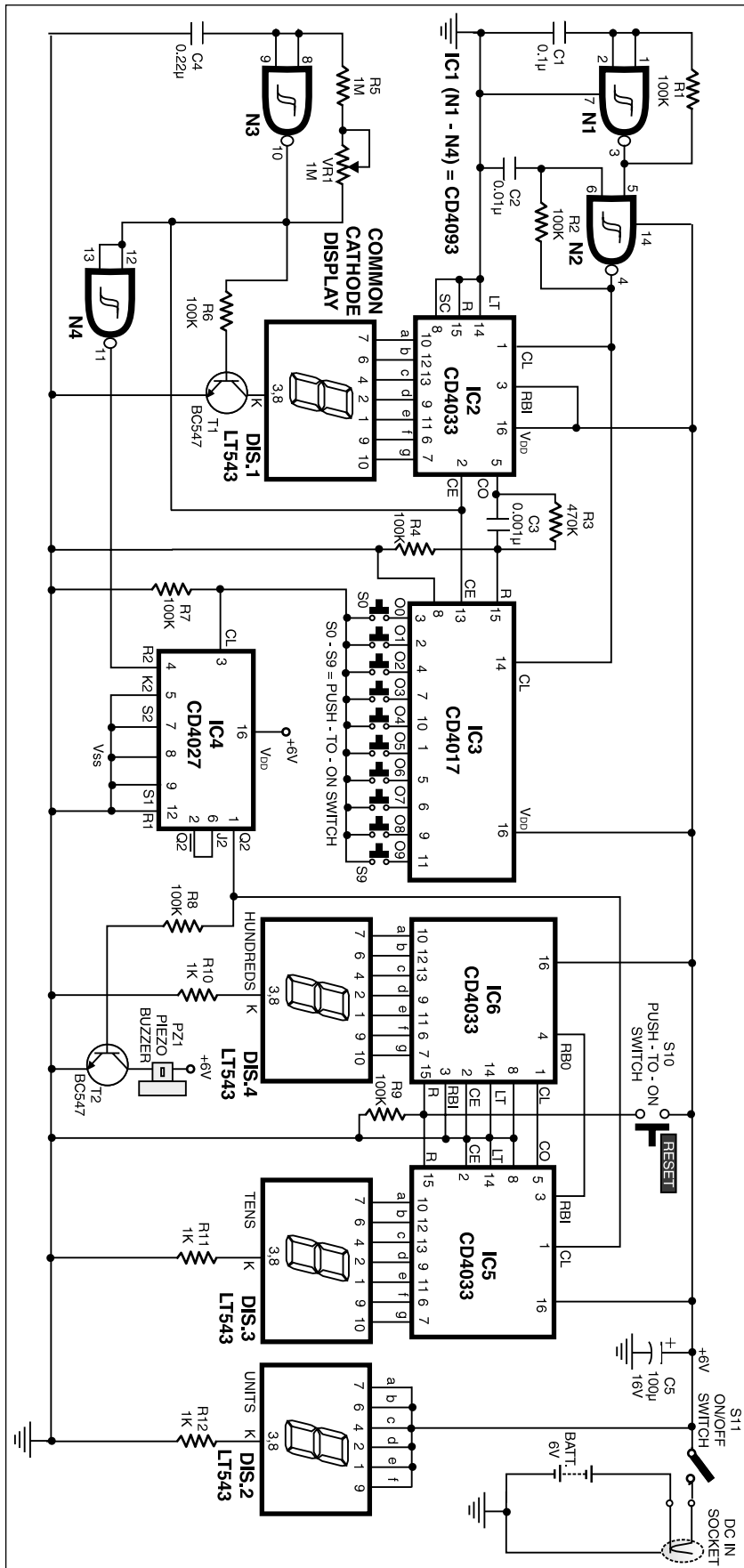


Fig. 2: Circuit diagram of the digital number shooting game



frequency (of the order of 1 Hz to 4 Hz). Its frequency can be varied with the help of potentiometer VR1.

For proper functioning of CD4033 and CD4017, their clock-enable (CE) pins 2 and 13 respectively must be held 'low'. These pins are connected to the output of gate N3 (pin 10). If these pins are in logic high state, the ICs are disabled from receiving clock pulses, and the Q outputs of IC3 and segment drive outputs of IC2 retain their last state before the CE pins go 'high'.

The control clock pulses from gate N3 also go to the base of transistor BC547B (T1). This transistor pulls down the common cathode of 7-segment LED display DIS.1 to ground during the high level of control clock pulses, to display the number.

The control pulse also performs one more function. After being inverted by NAND gate N4, it resets JK flip-flop IC CD4027 (IC4), which serves as the foul play checker.

In nutshell, during the low state of output of gate N3, both IC2 and IC3 are enabled and the pulses are counted by IC2, but the number cannot be seen in the display because transistor T1 is reverse biased and cut-off.

When the output of gate N3 changes to high state, IC2 and IC3 are disabled. T1 gets its base voltage and pulls down the cathode of display DIS.1, and the display shows the number (which is a random number). At the same time, the Q output of IC3 corresponding to the displayed number goes 'high'.

Now, if one presses the correct key corresponding to the number shown in the display, before it vanishes, a high-going pulse is applied to clock input pin 3 of IC4. Its Q output (pin 1) becomes 'high', which advances the tens counter (IC5 of the scoreboard). It also biases transistor T2, to drive the piezo buzzer PZ1 for confirmation of the number shot.

Foul play checker/debouncer. Due to bouncing, the switches produce spurious pulses and lead to erratic operation. The player may press a switch more than once to score more, and may keep pressing a switch before the respective number is displayed. This is where the foul play checker/debouncer circuit comes into play.

For faithful operation, the circuit requirements are as follows:

Fig. 3: Actual-size, single-sided PCB layout

Fig. 4: Component layout for the PCB

1. The spurious pulses must be ignored.
2. The counter must advance only on the first pressing of the switch for a number and further pressing must be ignored.
3. The pressing of the switch should be effected only after the corresponding number is displayed.

To fulfil all these conditions, the dual JK flip-flop IC CD4027 (IC4) is employed and only one of the two flip-flops is used. The flip-flop is inhibited when both J and K inputs are low (requirements 1 and 2). The data on the J input is transferred to the Q output for a positive-going clock pulse only (requirement 3). The K input (pin 5) of IC CD4027 is grounded and J input (pin 6) is connected to \bar{Q} output (pin 2). One terminal of all the ten switches is connected to clock input (pin 3) of IC4. Control pulses from gate N3 (pin 10) are inverted by gate N4 before it goes to

reset pin 4.

During the low-level period of gate N3, output of gate N4 is 'high' and the flip-flop (IC4) is in the reset state. If any one of the ten switches is pressed, even though clock pulses are present at clock input (pin 3) of IC4, the Q output will not change, as this IC is in the reset state.

When the output of gate N3 is 'high', the output of gate N4 is 'low', which clears IC4 from the reset state. If the player presses the correct switch, a clock pulse is applied to the clock input (pin 3) of IC CD4027. The 'high' level data from J input is transferred to Q output (pin 1) of this IC and IC5 advances by one count, which means ten points (DIS.2 is always zero). Now \bar{Q} output (pin 2) of IC4, which is connected to J input, goes 'low'. As both J and K inputs are at low level, IC4 is inhibited and further clock pulses to pin 3 of IC4 have no effect.

Score counter and scoreboard.

This block comprises two decade counter/decoder/7-segment display driver ICs CD4033 (IC5, IC6), and three common cathode 7-segment LED displays (DIS.2 through DIS.4). The 'a' through 'f' segments of DIS.1, meant for units, are directly connected to positive supply rail and its cathode is connected to negative supply rail through a 1k (R12) current-limiting resistor. Thus it always shows zero.

The Q output (pin 1) of IC4 is connected to clock input (pin 1) of IC5, the tens counter. The carry-out (pin 5) of IC5 is connected to the clock input (pin 1) of IC6 for cascading hundreds counter. The CE (pin 2) and Lamp Test (pin 14) of both IC5 and IC6 are grounded, for proper functioning. Both resets (pin 15) are grounded through a 100k (R9) resistor and connected to positive supply, through reset switch S10.

Ripple blanking input (pin 3) of IC6 is grounded, so the leading zero to be displayed in DIS.4 will be blanked out. The ripple blanking output (pin 4) will be low while the number to be displayed is zero. Likewise, zero will be blanked out in display DIS.3, because RB0 of IC6 is connected to RB1 of IC5. So when reset switch S10 is depressed, the unit counter display shows only zero and the other two displays are blanked out.

The maximum score which can be displayed is 1000, after which it automatically resets to zero.

Sound-effect generator. For simplicity and compactness, a piezo buzzer (continuous type) is employed. When the Q output of IC4 goes high, after the correct switch is pressed, it forward biases transistor BC547B (T2) and drives the piezo buzzer. This produces a beep sound for confirmation of successful shooting of that number.

Construction

This circuit can be assembled on a readymade PCB or strip board. However, a proper single-sided PCB for the circuit of Fig. 2 is shown in Fig. 3 and its component layout is shown in Fig. 4. For switches, push-to-on tactile or membrane switches can be used. For power supply, four pen-torch cells (AA3) can be used with a battery holder. DC IN socket is provided for connecting a battery eliminator for operating it on mains supply. □